

AUG-03-2004(TUE) 11:24 GALLAGHER & LATHROP

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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AUG 03 2004

Applicants: Masahiro Ishida, et al.

Serial No.: 09/699,077

Filing Date: October 27, 2000

Title: Method and Apparatus for
Fault Simulation of
Semiconductor Integrated
Circuit

Conf. No. 9031

Examiner: Ayal L. Sharon

Art Unit: 2123

OFFICIAL

August 3, 2004
San Francisco, California

Commissioner of Patents
P.O. Box 1450
Alexandra, VA 22313-1450

RESPONSE TO OFFICE ACTION

Sir:

This communication is submitted in response to the office action mailed May 3, 2004
(referred to herein as "Office Action").

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Docket: KPO089

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